REMARKS

Claims 1-49 are currently pending. Claims 1-49 are rejected. The title of the invention has been objected to. Claims 5-17, 19-20, 34-45, and 47-48 are objected to. Claims 1, 21, 29, 49 have been amended to clarify what is being claimed.

Title

The Examiner believes that the present title is not descriptive because it does not set forth what is new about the invention. Applicants respectfully disagree with the Examiner as to what the requirements are for the title of the invention. The present title describes what the invention is, namely, "A Flushable Free Register List." Applicants do not believe there is any requirement in either the MPEP or 37 CFR 1.72 that the Title of the Invention must set forth the novel aspect of the invention.

Claim Objections

Claims 5-17, 19-20, 34-45, and 47-48 are objected to. The Examiner has cited MPEP § 608.01 in support of this objection. Applicants respectfully choose to defer the renumbering of the claims until allowable subject matter is identified to avoid further confusion during prosecution. As such, Applicants respectfully request the Examiner to continue the objection until an indication of allowable subject matter.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-49 stand rejected under 35 USC 102(b) as being anticipated by Yeager (5,758,112). Applicants respectfully traverse this rejection on the basis of the above amendments and following arguments.

Summary of Yeager (5,758,112)

The Yeager reference is directed to redundant mapping tables for use in processors that rename registers and perform branch prediction is presented. The redundant mapping tables include a plurality of primary RAM cells coupled to a plurality of redundant RAM cells. In the event of a branch instruction, the redundant RAM cells can save the contents of the primary RAM cells in a

single clock cycle before the processor decodes and executes subsequent instructions along a predicted branch path. Should the branch instruction be mispredicted, the redundant cells can restore the primary RAM cells in a single clock cycle. A branch stack, coupled to the redundant mapping tables, updates restored mapping tables with changes made for preceding instructions that were decoded in parallel with the branch instruction. A plurality of levels of redundant RAM cells may be used to enable the nesting of a plurality of branch predictions at any one time.

Claims 1 and 29

Independent claims 1 and 29, as amended, are not anticipated by the Yeager reference because Yeager fails to disclose each and every element of claims 1 and 29. Specifically, Yeager fails to disclose at least two pointers set apart by a fixed distance and only move in unison up and down said structure. Examiner has admitted that Yeager does not disclose pointers that only move in unison.

Therefore, in view of the above amendments and arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claim 1 and 29 under 35 USC § 102.

Claims 21 and 49

Independent claims 21 and 49, as amended, are not anticipated by the Yeager reference because Yeager fails to disclose each and every element of claims 21 and 49. Specifically, Yeager fails to disclose providing a single structure to track register allocation for a first thread and a second thread of said multithreading microprocessor. Amended claims 21 and 49 now more clearly define that a single structure is provided to track register allocation for a first thread and a second thread. Yeager does not disclose a single structure as claimed in claims 21 and 49.

Therefore, in view of the above amendments and arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claim 21 and 49 under 35 USC § 102.

Claims 22 and 28

Independent claims 22 and 28 are not anticipated by the Yeager reference because Yeager fails to disclose each and every element of claims 22 and 28. Specifically, Yeager fails to disclose a retire row pointer to identify where a pointer pointing to said physical register on an instruction in said first thread is next to be retired. The graduation mask in Yeager indicated by the Examiner is not a retire pointer to identify where a pointer pointing to said physical register of an instruction in said first thread is next to be retired. The Yeager reference discloses both pointers and masks. In fact, Yeager discloses a system with both a write pointer and a write mask. Thus pointers and masks as disclosed by Yeager are not the same thing, nor do they serve the same purpose or function in the same manner. Furthermore, even if one adopts the Examiner's interpretation that the graduation mask of Yeager is a pointer under a broad dictionary definition. The graduation mask of Yeager does not "identify where a pointer pointing to said physical register of an instruction in said first thread is next to be retired." The Examiner has admitted that the graduation mask of Yeager indicates a row in a group. While this may indicate which instructions graduate it does not identify where a pointer pointing to said physical register of an instruction in said first thread is next to be retired.

Therefore, in view of the above amendments and arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claim 22 and 28 under 35 USC § 102.

Claims 2-20 and 30-48

Claims 2-20 and 30-48 depend either directly or indirectly from claims 1 and 29 respectively and as such incorporate each and every element of their respective independent claims. As discussed above Yeager fails to disclose each and every element of claims 1 and 29. As such Yeager fails to teach each and every element of claims 2-20 and 30-48.

Further dependent claim 2 and 30, and subsequently claims 5, 9, 10, 11, 13, 15, 17, 20, 30, 33, 37-39, 41, 43, 45, and 48 that depend directly or indirectly from claims 2 or 30, further recite tracking a second thread in the structure. As such, the deficiencies of Yeager discussed above in

regard to claims 21 and 49 also apply because Yeager fails to disclose a single structure for tracking a first and second thread.

Dependant claims 4 ,5, 32, and 33, and subsequently claims 6-17, 19, 20, 34-45, 47, and 48 that depend directly or indirectly from claims 4, 5, 32, or 33, further recite a retire pointer. For the reasons discussed above in regard to claims 22 and 28, the Yeager reference does not disclose a retire pointer.

Therefore, in view of the above amendments and arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 2-20 and 30-48 under 35 USC § 102.

Claims 23-27

Claims 23-27 depend either directly or indirectly from claim 22 and as such incorporate each and every element of claim 22. As discussed above Yeager fails to disclose each and every element of claim 22. As such Yeager fails to teach each and every element of claims 23-27.

Therefore, in view of the above amendments and arguments, Applicants respectfully requests the reconsideration and withdrawal of the rejection to claims 23-27 under 35 USC § 102.

CONCLUSION

In view of the remarks set forth above, Applicants believe that the present invention is in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

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Respectfully submitted,

By _____

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